RF and Mechanical Characterization of Flip-Chip Interconnects in CPW Circuits with Underfill

Zhiping Feng, Wenge Zhang, Bingzhi Su, K. C. Gupta, *Fellow, IEEE,* and Y. C. Lee

***Abstract*— RF characterization of flip-chip interconnects in coplanar waveguide (CPW) circuits with underfill is reported. The scattering-parameters have been measured up to 40 GHz for GaAs CPW through-line chips flip-chip mounted on an alumina substrate with and without an underfill epoxy. A lumped-element model of flip-chip interconnect has been developed for flip-chip assemblies with and without epoxy. Fatigue life of flip-chip assemblies has been computed for different chip sizes and substrates. The results show feasibility of using underfill encapsulant in microwave/millimeter-wave frequency range.**

***Index Terms*—CPW circuits, flip-chip, mechanical characterization, RF characterization.**

I. Introduction

BECAUSE of several advantages compared to wire bonding (low cost, better performance, high reliability, etc.), RF and microwave assembly packages are increasingly likely to use flip-chip bonding instead of wire bonding [1]. Generally, flip-chip assembly requires an underfill to reduce the stress on joints during thermal excursions, to increase the fatigue life of joints, and to protect the assembly from environment [2]–[7]. However, the underfill material affects the electrical performance of the assembly due to different values of its dielectric constant and dissipation factor $(\tan\delta)$ compared to those of air. The only related study reported earlier is of the effect of Sealgard $(\varepsilon_r = 2.8)$ and Globtop $(\varepsilon_r = 3.14)$ on performance of a low-noise amplifier (LNA) in the frequency range from 5–15 GHz [8]. In this paper, both electrical and mechanical characterizations of coplanar waveguide (CPW) flip-chip assemblies with underfill encapsulant have been reported. The effects of underfill encapsulant on RF performance are characterized up to 40 GHz based on measurements on CPW flip-chip assemblies. A lumped-element model of flip-chip interconnects has been developed for flip-chip assemblies with and without epoxy. Reliability analysis of flip-chip assemblies has been carried out by finite element analysis (FEA) and results for the fatigue life are presented.

II. Test Circuits and Assembly

Two GaAs chips containing CPW through-line sections and on-wafer probe pads were selected for this experiment [9]. Chip #1, with dimensions of 1.106 mm × 1.380 mm × 0.635 mm, has a 50-Ω CPW through line of 0.600 mm length fabricated on it. Chip #2, with length of 4.700 mm, is longer than chip #1 and has a 4.125-mm CPW line on it. On these test chips, six silver bumps were plated at the ends of the CPW line and on the edges of ground planes. The dimension of the bumps is 75 μm in height and 150 μm in diameter before bonding. Multiline-TRL calibration set [10] and the circuits for mounting GaAs chips were designed using 50-Ω CPW transmission lines and fabricated on a single 25.4 mm × 25.4 mm alumina substrate. Fig. 1 shows the circuit layout fabricated on the alumina substrate.

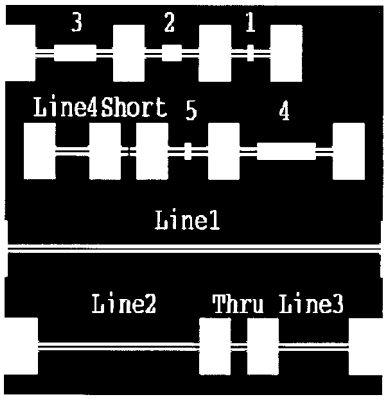

Fig. 1. Layout of calibration standard set and carrier circuits on alumina substrate.

The GaAs chips were mounted on the alumina substrate by thermosonic flip-chip bonding [11]. The parameters selected for this operation were: temperature 180 °C, bonding force 1.575 kg, and ultrasonic power 8.5 W. After bonding, the epoxy (U300 from Epoxy Tech. Inc., with $\varepsilon_r = 4.1$ and $\tan\delta = 0.009$ at 100 KHz) was filled in the gaps between chips and the substrate and cured at 120 °C for 25 min.

RF measurements were performed on an HP8510 network analyzer with on-wafer probes for a frequency range 0.05–40 GHz. Measurements on assemblies for chip #1 and chip #2 were carried out before as well as after adding the underfill encapsulant.

III. RF Measurement Results and Characterization

Figs. 2 and 3 show measured S-parameters of the flip-chip assembly for chip #1 with and without underfill as a function of frequency, and Figs. 4 and 5 show similar results for the assembly with chip #2. Comparing the measured results of the two flip-chip assemblies with and without underfill, we see three kinds of effects due to underfill: 1) the return loss and insertion loss of flip-chip assemblies increase; 2) the

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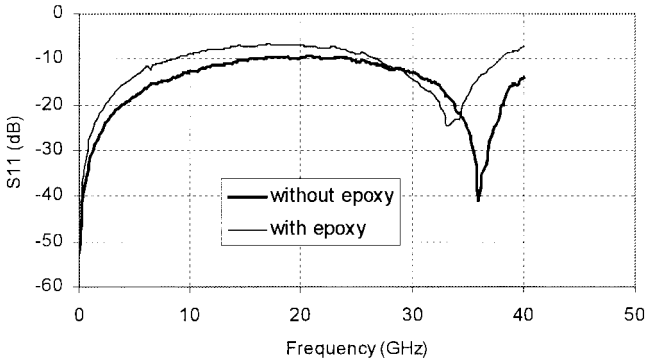


Fig. 2. Comparison of measured S_{11} of flip-chip assembly with and without underfill epoxy for chip #1.

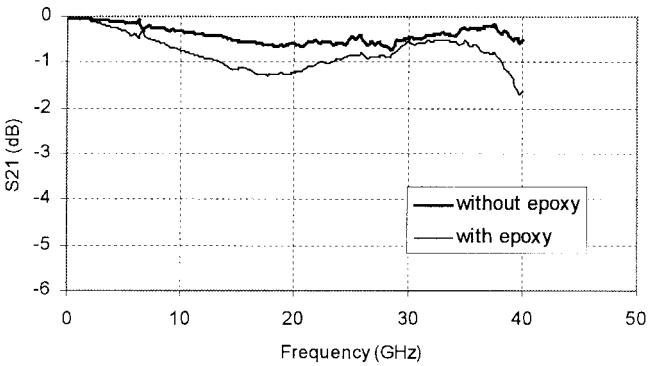


Fig. 3. Comparison of measured S_{21} of flip-chip assembly with and without underfill epoxy for chip #1.

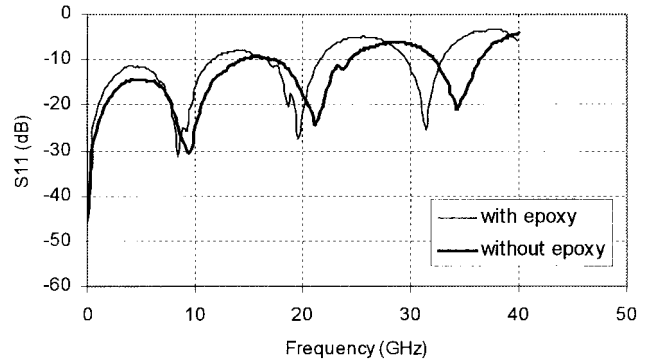


Fig. 4. Comparison of measured S_{11} of flip-chip assembly with and without underfill epoxy for chip #2.

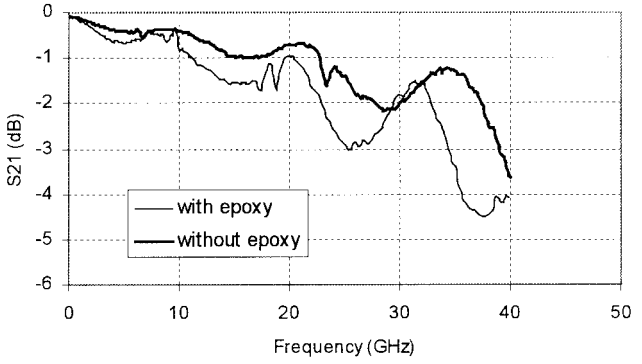


Fig. 5. Comparison of measured S_{21} of flip-chip assembly with and without underfill epoxy for chip #2.

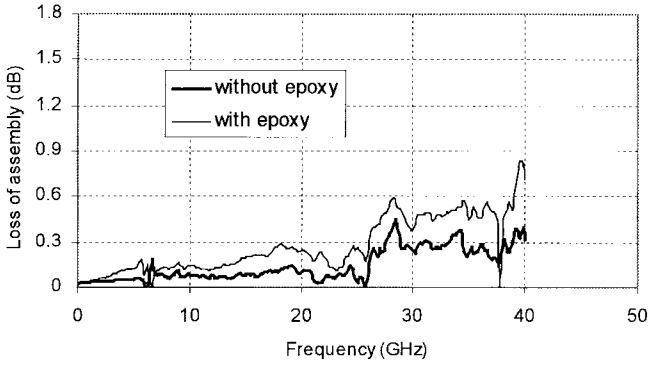


Fig. 6. Comparison of losses of flip-chip assemblies for chip #1 with and without underfill epoxy.

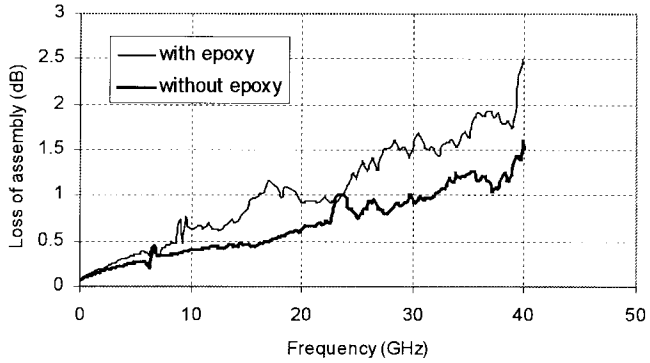


Fig. 7. Comparison of losses in flip-chip assemblies for chip #2 with and without underfill epoxy.

frequencies of minimum reflection shift downwards; and 3) the phase of the transmission coefficient shifts due to the epoxy.

A. Losses

The loss in the flip-chip assembly includes the loss of the CPW line on the alumina substrate, the loss of the CPW line on the GaAs chip, and the loss of flip-chip joints. After addition of the underfill material, the presence of epoxy increases the loss. Figs. 6 and 7 show the loss (evaluated as $10\log\{(1-(S_{11})^2)/(S_{21})^2\}$) of the flip-chip assemblies with and without underfill epoxy for chip #1 and chip #2, respectively, as functions of frequency. The additional loss at 40 GHz due to underfill epoxy is less than 0.6 dB (0.266 dB/mm) for the flip-chip assembly with chip #1 and less than 1 dB (0.213 dB/mm) for the flip-chip assembly with chip #2.

B. Change in ε_{re} of CPW Line on GaAs

The shift in frequencies of minimum reflection can be attributed to the difference in the values of effective dielectric constant of CPW with and without the underfill epoxy. Effective dielectric constants of CPW on GaAs with and without underfill (as computed by EM simulations on HP-HFSS, a full-wave EM simulator-based finite element electromagnetic analysis) are 7.259 and 8.917, respectively. The difference caused by the underfill is about 23%. Table I shows the measured and calculated (using the computed values of the

TABLE I
COMPARISON OF MEASURED AND CALCULATED FREQUENCIES FOR MINIMUM REFLECTION IN FLIP-CHIP ASSEMBLIES WITH UNDERFILL EPOXY

No. of chip	Frequency at minimum reflection (GHz)		
	Measured without epoxy	Measured with epoxy	Calculated with epoxy
Chip#1	36.0050	32.2085	32.4857
Chip#2	34.2073	31.4108	30.8637
Chip#2	21.2235	19.6255	19.1490
Chip#2	9.4383	8.4385	8.5157

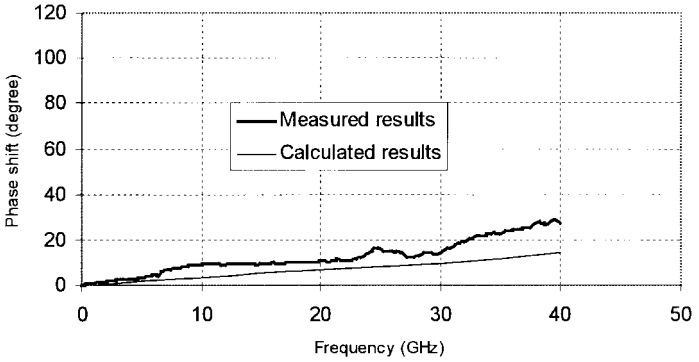


Fig. 8. Comparison of measured and calculated phase shifts for chip #1 with and without epoxy.

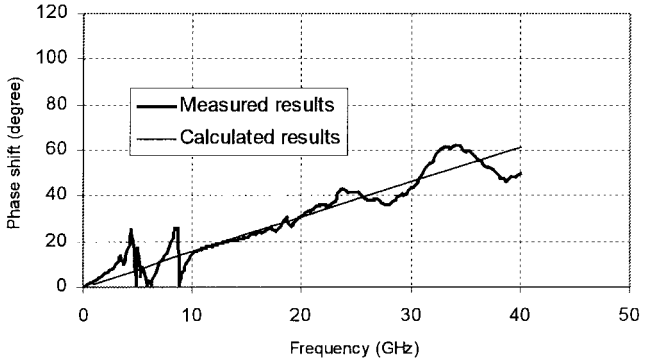


Fig. 9. Comparison of measured and calculated phase shifts for chip #2 with and without epoxy.

effective dielectric constants) frequencies of minimum reflection for the two assemblies. The good agreement between the measured and calculated frequencies for minimum reflection validates the accuracy of our measurements and modeling.

C. Phase Shift Due to Underfill Epoxy

The phase shift of the transmission coefficient S_{21} before and after adding the epoxy underfill consists of three parts: the first and the major part is the phase shift in CPW on GaAs with and without epoxy (about 10.50° for chip #1 and 59.85° for chip #2 at 40 GHz), the second part is phase shift due to bump interconnects (about 3.05° at 40 GHz), the third part is phase shift in CPW line on alumina (about 0.66° at 40 GHz). The bump height after bounding is about 62 μm, and the length of CPW on alumina that got covered by epoxy is about 150 μm. The measured and calculated values of phase shifts for chip #1 and chip #2 are shown in Figs. 8 and 9. There is a fair agreement between the measured and calculated phase shifts.

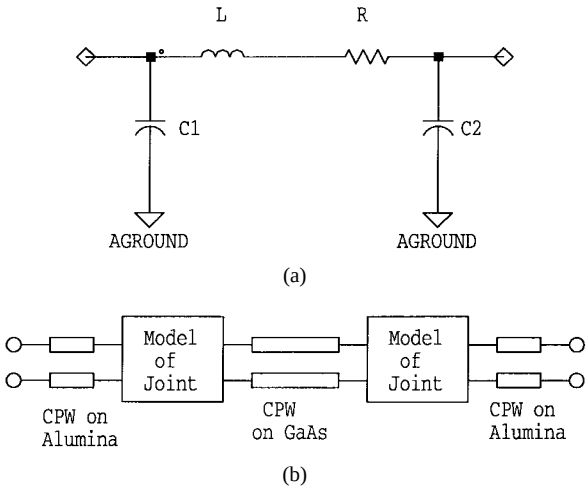


Fig. 10. Modeling of CPW flip-chip interconnects. (a) The lumped-element model for CPW flip-chip interconnects. (b) Schematic of flip-chip assembly used for modeling in MDS.

IV. MODELING BASED ON MEASURED RESULTS

A lumped-element circuit model for a single CPW flip-chip interconnect, a set of three bumps (not the assembly of a through-line with two interconnects at two ends), is developed based on physical considerations and is shown in Fig. 10(a). In this model, L denotes the inductance of bumps. $C1$ and $C2$ represent the discontinuity capacitances at the bumps' locations on alumina and GaAs substrates, respectively. R denotes the loss in the flip-chip interconnect. Values of various elements in this model are derived by comparing S-parameters of the interconnects assembly with the measured results. The assembly considered for the comparison consists of a CPW through-line on GaAs, two interconnect models on each side and two short sections of CPW line on alumina as shown in Fig. 10(b). For CPW on GaAs, the effect of alumina substrate on Z_0 and ε_{re} with and without epoxy are evaluated by EM simulation using HP-HFSS. The initially assumed values of the lumped elements in the model are varied by the optimization tool in microwave design system (MDS). Optimized values corresponding to the lowest differences between measured S-parameters and those obtained from network analysis on MDS are the values of L, R, $C1$, and $C2$ for the model shown in Fig. 10.

The lumped-element models used for flip-chip interconnects with and without epoxy are identical; however, the values of elements in the model for flip-chip interconnects with and without epoxy are different. Figs. 11 and 12 show the comparison between measured S-parameters and the corresponding responses using the lumped-element model for chip #1 without underfill epoxy. We note that model agrees very well with the measured results. The corresponding value of model parameters are shown in Table II. Figs. 13 and 14 show similar results for chip #1 with underfill epoxy. Again, there is good agreement between measured results and the response of the model. These model values are also shown in Table II. The values of inductances in both cases are very close. Values of two capacitances increase when underfill epoxy is added. Using the lumped-element circuit model, we

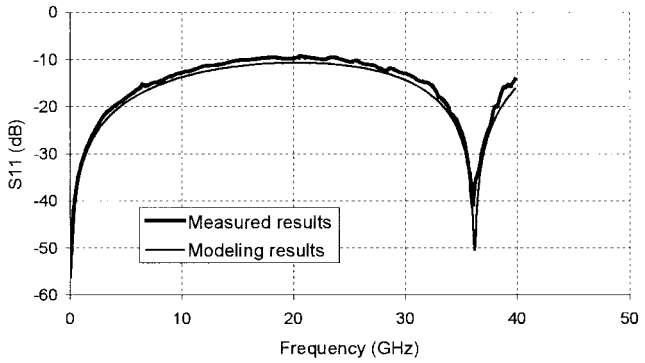


Fig. 11. Comparison of measured S_{11} and the model of the flip-chip assembly for chip #1 without epoxy.

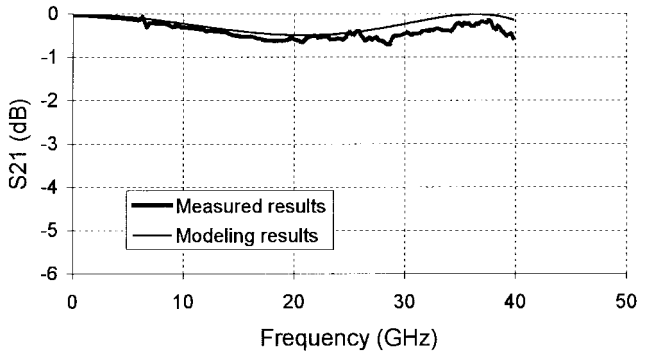


Fig. 12. Comparison of measured S_{21} and the model of the flip-chip assembly for chip #1 without epoxy.

TABLE II
VALUES OF VARIOUS ELEMENTS IN THE MODEL OF FLIP-CHIP INTERCONNECT WITH AND WITHOUT EPOXY

	L (nH)	R (Ω)	C1 (pF)	C2 (pF)
Chip #1 w/o epoxy	0.014	0.018	0.081	$2x10^{-5}$
Chip #1 with epoxy	0.010	0.028	0.011	$1.2x10^{-4}$

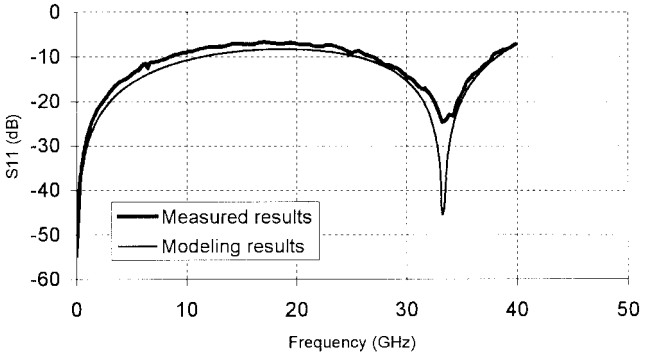


Fig. 13. Comparison of measured S_{11} and the model of the flip-chip assembly for chip #1 with epoxy.

can calculated the insertion loss introduced by a single CPW flip-chip interconnect (set of three bumps). The increase in the insertion loss because of underfill epoxy is found to be 0.5 dB at 35 GHz.

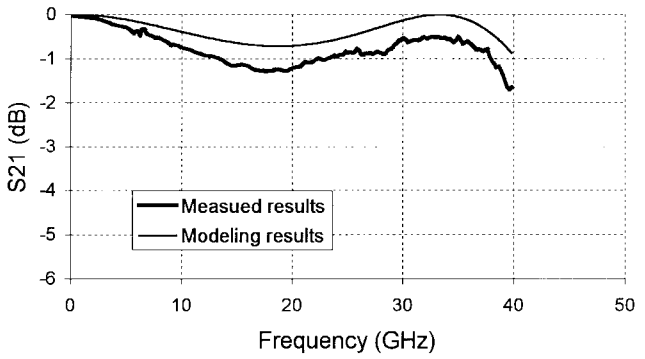
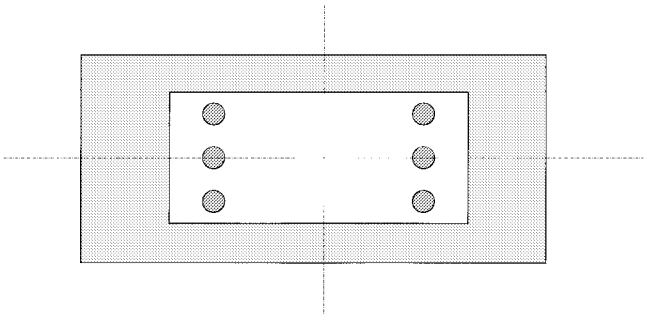
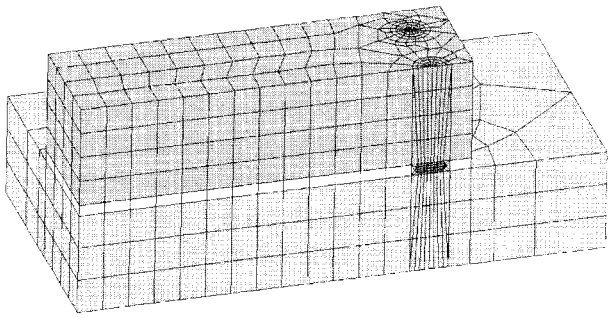


Fig. 14. Comparison of measured S_{21} and the model of the flip-chip assembly for chip #1 with epoxy.



(a)



(b)

Fig. 15. The structure for the finite element analysis of flip-chip assembly. (a) Top view of the structure. (b) The mesh for the finite element analysis of the flip-chip assembly.

V. MECHANICAL CHARACTERIZATION OF FLIP-CHIP ASSEMBLY WITH UNDERFILL ENCAPSULANT

Thermomechanical stresses on the joints, due to coefficient of thermal expansion (CTE) mismatch between the flipped chip and the substrate, lead to thermomechanical fatigue and consequent failure of the assembly. This stress can be reduced by encapsulation of the joint with an underfill encapsulating material. This enhances the reliability of the assembly. Computations leading to fatigue life consist of three steps: 1) solder joint profile prediction; 2) evaluation of inelastic strain energy density by using FEA; and 3) fatigue life estimation. The solder joint profile was obtained by using Surface Evolver (a software for predicting solder joint profile developed by University of Minnesota), and the details of this model can be found in [13]. The other two steps are described below.

Fig. 15 shows the mesh for the FEA of the assembly with underfill epoxy. Because of the symmetry, only 1/4

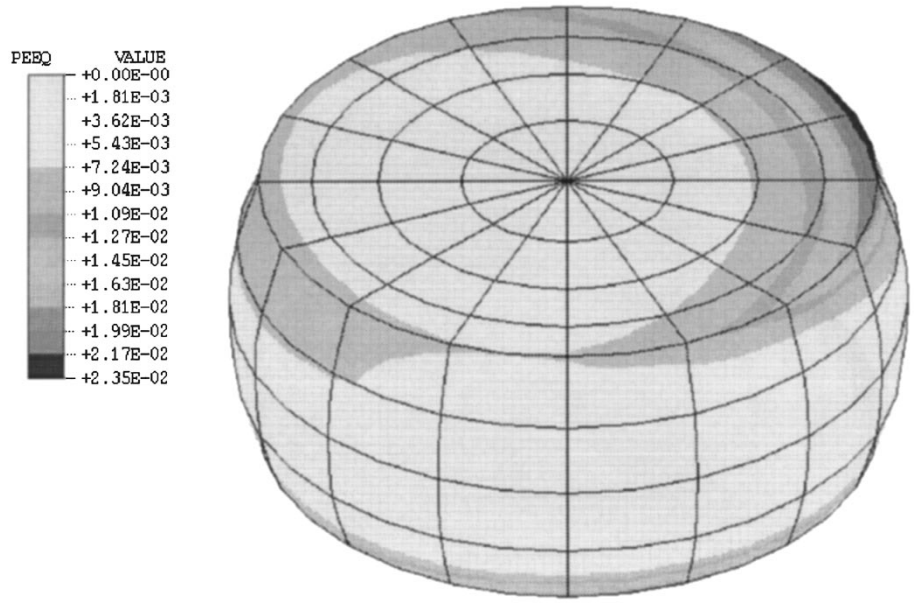


Fig. 16. The distribution of equivalent plastic strain in the solder joint.

TABLE III
MECHANICAL PROPERTIES FOR FEM SIMULATION

Properties	CTE (10^{-6}/K)	Modulus (Mpa)	Tg (°C)
GaAs	5.7	112815	
Epoxy(U300)	105	7500	130
Duroid	17	2070	
Ceramic(Al_2O_3)	5.6	372384	

of the assembly was analyzed. Typically, the finite element deformation/strain/stress analysis for flip-chip or ball grid array (BGA) assemblies uses global and local models [13]. In the present case, since the number of joints is only six, it is possible to merge the global model and local model into one for computational efficiency. In this model, the 20-node quadratic brick element and 15-node quadratic triangular prism element were used for thermally induced strain/stress/fatigue analysis. There are four layers of elements in the solder joint (Fig. 16). The model was established using Patran 3, and the computation used Abaqus 5.6.[1] The material properties, coefficient of thermal expansion (CTE), Young's modulus, and glass transition temperature (T_g) are listed in Table III. The plastic properties of solder joint were taken from [13]. The results obtained from the model were strain/stress distributions and the maximum inelastic strain energy density in the solder joint. The maximum inelastic strain energy density was used to estimate the fatigue life of solder joint.

For estimation of the fatigue, the inelastic strain energy density method was chosen [14]. The cyclic inelastic strain energy density (ΔW) calculated by FEA was used as the failure indicator. ΔW was correlated with thermal cycles for crack initiation and propagation. Since the elastic strain energy was recoverable, only plastic and creep strain energy densities were used in the estimation. The accumulated inelastic strain energy reached a stable level after the second cycle, so the local model calculated only two thermal cycles. The maximum energy density of the second cycle was used for estimation of solder fatigue life. The inelastic strain energy density ΔW is defined as

$$\Delta W = \int_C \tau_{ij}\, d\varepsilon_{ij}^P + \int_C \tau_{ij}\dot{\varepsilon}_{ij}^C\, dt \tag{1}$$

where τ_{ij} are the stress components, $d\varepsilon_{ij}^P$ are the incremental plastic strain components, and $\dot{\varepsilon}_{ij}^C$ are the creep strain rate components. The integrals in (1) are carried over one thermal cycle denoted by c. The empirical relations developed by Daveaux [6] for crack initiation and propagation in eutectic Sn–Pb solders are

$$N_0 = 7860\Delta W^{-1.0} \tag{2}$$

$$da/dN = 4.96 \times 10^{-8}\Delta W^{1.13} \tag{3}$$

where N_0 is the number of cycles before a crack forms, and da/dN is the area crack growth rate. The unit for ΔW is psi. The numbers of cycles of the solder fatigue is estimated as

$$N_f = N_0 + a/(da/dN) \tag{4}$$

where a is crack length of the solder joint in inches and this length is chosen as 1.5 times the pad diameter.

In the present study, the solder pad diameter selected is 150 μm, and the solder height is 62 μm. The die thickness is 635 μm, and the substrate thickness is 635 μm. Eight cases are selected (see Table IV) to study the effects of die size, substrate material, and underfill epoxy on the fatigue life of solder joints. The fatigue analysis is based on the thermal cycling with temperature changes from 0 °C to 100 °C with 240 s dwell time and 150 s ramp time. Fig. 16 shows the plastic equivalent strain distribution of the solder joint at the corner of the die. It can be seen that the maximum plastic equivalent strain is at the upper right-hand corner of the solder joint, and this is consistent with the experimental observation that cracks always start here for a convex shape joint.

Fig. 17 shows the values of the fatigue life for the eight cases listed in Table IV. Without underfill epoxy, the fatigue

[1] Patran 3 and Abaqus 5.6 are FEA softwares which are available from PDA Engineering and Hibbitt, Karlsson & Sorensen Inc., respectively.

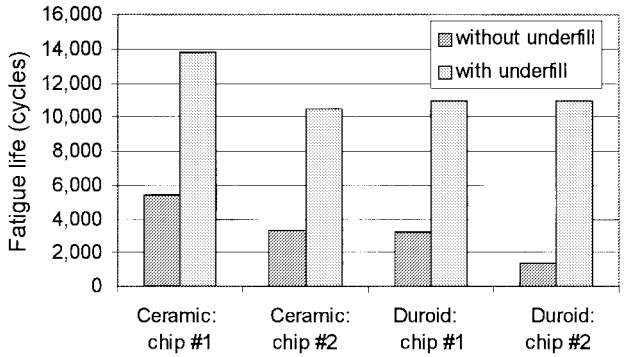


Fig. 17. Fatigue life of different assemblies.

TABLE IV
EIGHT CASES CONSIDERED FOR COMPUTING FATIGUE LIFE OF FLIP-CHIP JOINTS

Case	Dies	Material of substrate	With/without Underfill epoxy
1	Chip #1	Ceramic	Without
2	Chip #2	Ceramic	Without
3	Chip #1	Duroid	Without
4	Chip #2	Duroid	Without
5	Chip #1	Ceramic	With
6	Chip #2	Ceramic	With
7	Chip #1	Duroid	With
8	Chip #2	Duroid	With

life of the assembly with duroid substrate and die size of 4.700 mm $\times$ 1.389 mm (chip #2) is only 1300 cycles. The fatigue life of the assembly with alumina ceramic substrate is 3300 cycles. The duroid substrate decreases the fatigue life greatly. The duroid substrate leads to a larger global mismatch on solder joint due to its larger CTE (17 ppm) compared with that of alumina (5.6 ppm). For the assembly on the duroid substrate and without the underfill epoxy, the fatigue life is too small to be acceptable. In order to increase the reliability and the fatigue life of the assembly, an underfill epoxy is needed. As shown in Fig. 17, the underfill epoxy increases the fatigue life of the assembly with chip #2 on the duroid substrate from 1300 to 11 000 cycles. The underfill epoxy reduces the global mismatch of solder joints and leads to a longer fatigue life of solder joints. The effect of underfill epoxy in this case is very impressive.

VI. CONCLUDING REMARKS

The investigations reported in this paper show that the U300 epoxy (from Epoxy Tech. Inc.) with $\varepsilon_r = 4.1, \tan\delta = 0.009$ (measured at 100 kHz) can be used for flip-chip assemblies up to 40 GHz with only a small additional loss. The effect of the change in ε_{re} can be compensated by modifying the line lengths appropriately. By choosing an underfill epoxy with lower loss and lower dielectric constant, the effects of underfill could be reduced further. The underfill epoxy does not change the lump-element model of the flip-chip interconnect greatly and increases the insertion loss of one flip-chip interconnect by 0.5 dB at 30 GHz. Underfill encapsulant increases the fatigue life of flip-chip assemblies significantly.

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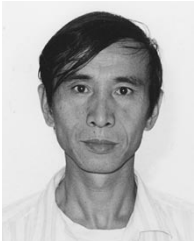

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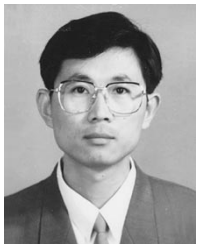

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